Adaptive Design of FPGA-based Direct Digital Frequency Synthesizer to Optimize Angular Precision and Amplitude Precision

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Abstract— **A Direct Digital Frequency Synthesizer designed core is implemented and validated in this paper. This electronics paper proposed the details of programming model optimal and feasible architecture of Direct Digital Synthesizer that eliminates the need for the manual tuning and tweaking related to component aging and temperature drift in analog synthesizer solutions. A Direct Digital Synthesizer play a vital role in Digital frequency Down Conversion in such an application, the DDC (Digital Down converter) has become a cornerstone technology in communication systems. Here, the design of Digital Frequency Synthesizer gives an output with specified frequency and phase which is adjustable at runtime. This paper also evaluates the performance of DDS under various programming parameters and the performance is implemented on Virtex II Pro.**

Index Terms—**Direct Digital Frequency Synthesizer, Performance of Digital Frequency Synthesizer, Design Approach, Simulation Results.**

I. Introduction

The DDS (DDS synthesizer) is an implementation of a direct digital frequency synthesizer (DDS) which produces a sine wave at the output with a specified frequency and phase (adjustable at run time).

DDS technique makes arbitrary periodical waveform generation possible as well as a sine wave generation. If the arbitrary periodical waveform sample values are loaded into the internal look-up table module in the DDS, the arbitrary periodical waveform with desired frequency and phase can be generated. These synthesizers can generate lower frequencies but, they allow fine step sizes and more accurate frequency values.

II. Direct Digital Synthesizer

The direct frequency synthesizers use DDS technique which lets generating sine waves at very precise frequencies [1, 2]. As the name implies, the analog sine wave is completely generated by digital circuits in this technique. The digitally quantized samples of the desired waveform are generated at the input reference clock frequency. The generated digital samples of the waveform are converted to analog signals using the D/A converters and filter circuits.

The resolution of the Frequency Tuning Word (FTW), the phase and the amplitude are defined separately. While the FTW resolution can be set by the generic ftw_width, phase and amplitude resolution are defined as constants phase_width and ampl_width in the separate package sine_lut_pkg. This is generated by a matlab script (sine_lut_gen.m); the m-files are described in their headers. The nomenclature of the files is sine_<phase_width>_x_<amplitude_width>_pkg.vhd. By adding one of these files to the project, the resolution of phase and amplitude is automatically defined.

Figure1 shows a block diagram of the implemented DDS synthesizer. The signals clock and reset are not shown here. The resolution parameters have been renamed (ftw_width = N, phase_width = M, and amplitude_width = P). Only the first period of the sine wave is stored in the LUT, the two most significant bits of the phase word are used either to shift the input value or to invert the output amplitude, depending on the quadrant of the sine wave. The LUT is clocked, so the total delay from input to output is 3 clock cycles.

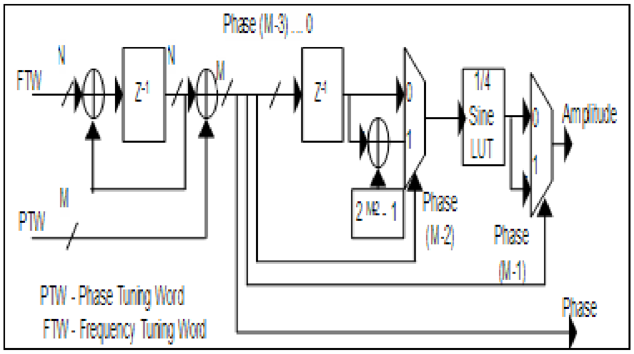

Figure 1: Block diagram of DDS implementation

The output frequency will be determined by the FTW.

$\mathbf{F}_{\mathbf{dds}} = (FTW/2^{(N-M)})*(F_{clk} / (2^{M}))$ or

$\mathbf{F}_{\mathbf{dds}} = FTW*F_{clk}/2^{N}$

Where F_{clk} = Clock Frequency

The initial phase can be controlled by PTW.

$\mathbf{\Phi}_{\mathbf{dds}} = (PTW/2^{M})*2*pi$

A. FTW bit width calculations

It is determined using minimum frequency change required If we simplify the equation

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$\mathbf{F}_{\mathbf{dds}}$ = FTW/$2^{(N-M)}$)*(F_{clk}/ (2^M))
$\mathbf{F}_{\mathbf{dds}}$ = FTW*F_{clk}/ ($2^N * 2^{-M} * 2^M$)
$\mathbf{F}_{\mathbf{dds}}$ = FTW*F_{clk}/2^N
FTW = 1 for minimum frequency change and
Minimum frequency change = 1e3 Hz
So, 1e3 = 1*50e6/2^N
N = 15.6096 H” 16
The FTW width should be 16 bits.

B. *PTW bit width calculations*

It is determined using the minimum frequency required at the output.

- If the min frequency change required and the minimum frequency required are same then PTW bit width = FTW bit width i.e. M = N.
- If they are not same then;

M = $\log_{10}$ ((F_{clk}/min_Freq))/$\log_{10}$ (2)
Let min_Freq = 5e3 Hz
M = $\log_{10}$ ((F_{clk}/5e3))/$\log_{10}$ (2)
M = 13.2877 H” 13

C. *Advantages of DDS*

- DDS performance allows for very fast frequency switching at a stumpy rate.
- Waveform frequency is digitally runtime adjustable with micro hertz frequency resolution.
- The waveform phase and amplitude can be adjusted digitally.
- The DDS core can be combined with additional signal processing blocks to make clock generators.

III. Simulation Results

A. Performance of DDS at different Frequencies

Parameters used for DDS module:
Sampling Frequency: 60 MHz
Frequency Tuning Word: 11bit
Phase Tuning Word: 9 bit
Output Amplitude Tuning Word: 16 bit
The design parameters are assigned in Matlab using text file which can be read out by testbench from ISE. The suitable design parameter for DDS module is assigned in table I.

Table I: Performance parameter of DDS

Frequency Required	FTW	FTW Actual	Frequency Generated	Actual Frequency from Simulation
750KHz	25.6	26	762KHz	762KHz
2MHz	68.266	68	1.99MHz	1.99MHz
5MHz	170.661	171	5.00MHz	5.00MHz
20MHz	682.66	683	20.009MHz	20.032MHz

In this paper, designed Direct Digital Frequency Synthesizer module VHDL code is implemented into Xilinx FPGA, output are displayed using MATLAB and debugged the module on hardware platform with Chipscope pro.

Implementing a DDS having various periodical waveform creation capability at different frequency, result shown in figure 2, 3, 4 & figure 5. Periodical waveform generation is a key function for all communication systems. The performance of Direct Digital Frequency Synthesizer is controlled by Frequency Tuning Word (FTW). Implementing a DDS having various periodical waveform creation capability at different frequency, result shown in figure 2, 3, 4 & figure 5. Periodical waveform generation is a key function for all communication systems. The performance of Direct Digital Frequency Synthesizer is controlled by Frequency Tuning Word (FTW).

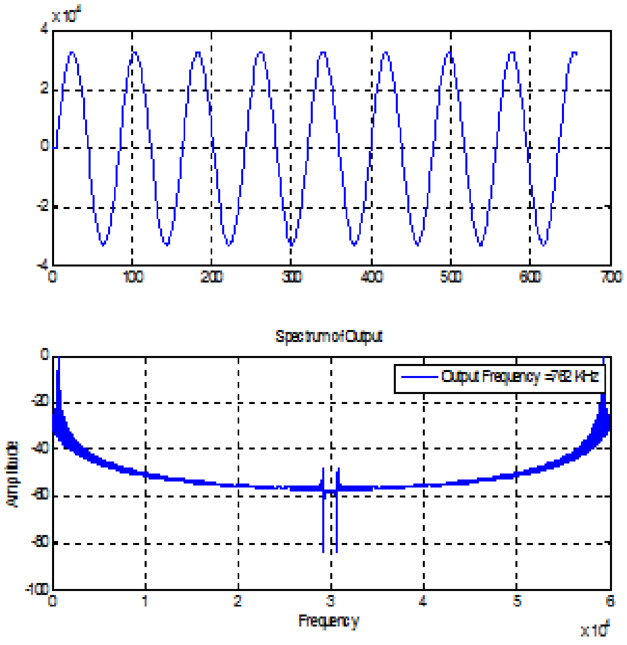

Figure 2: DDS Output at 750 KHz

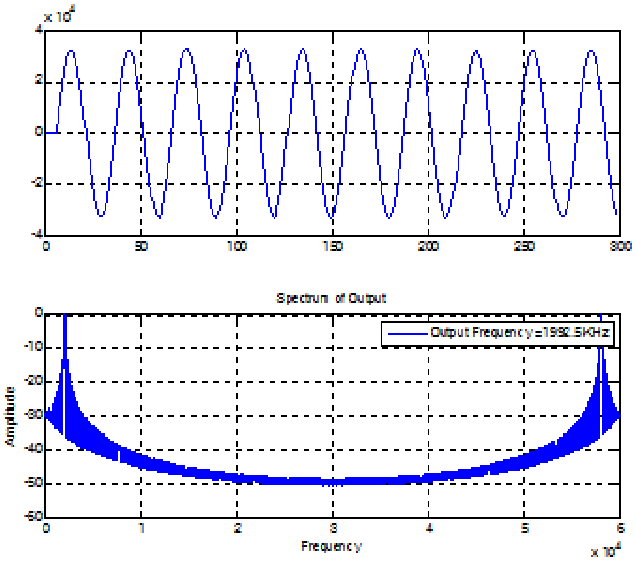

Figure 3: DDS Output at 2 MHz

B. Simulation and Verification of DDS at Fixed Frequency

Table II: Frequency and FTW Parameter of DDS

Frequency Required	FTW	FTW Actual	Frequency Generated	Actual Frequency from Simulation
5MHz	170.661	171	5.00MHz	5.00MHz

The phase and frequency of designed Direct Digital Frequency Synthesizer is adjustable at runtime also and for a

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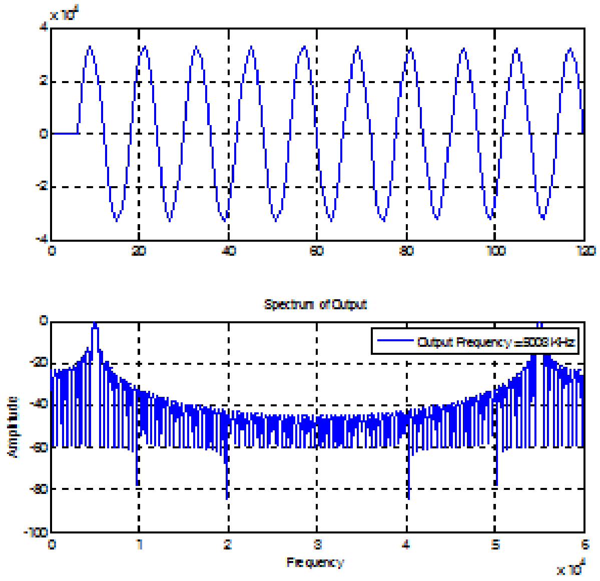


Figure 4: DDS Output at 5 MHz

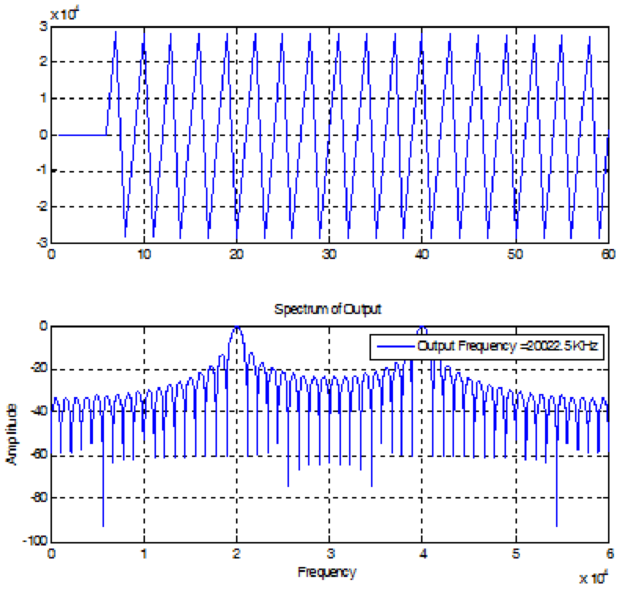
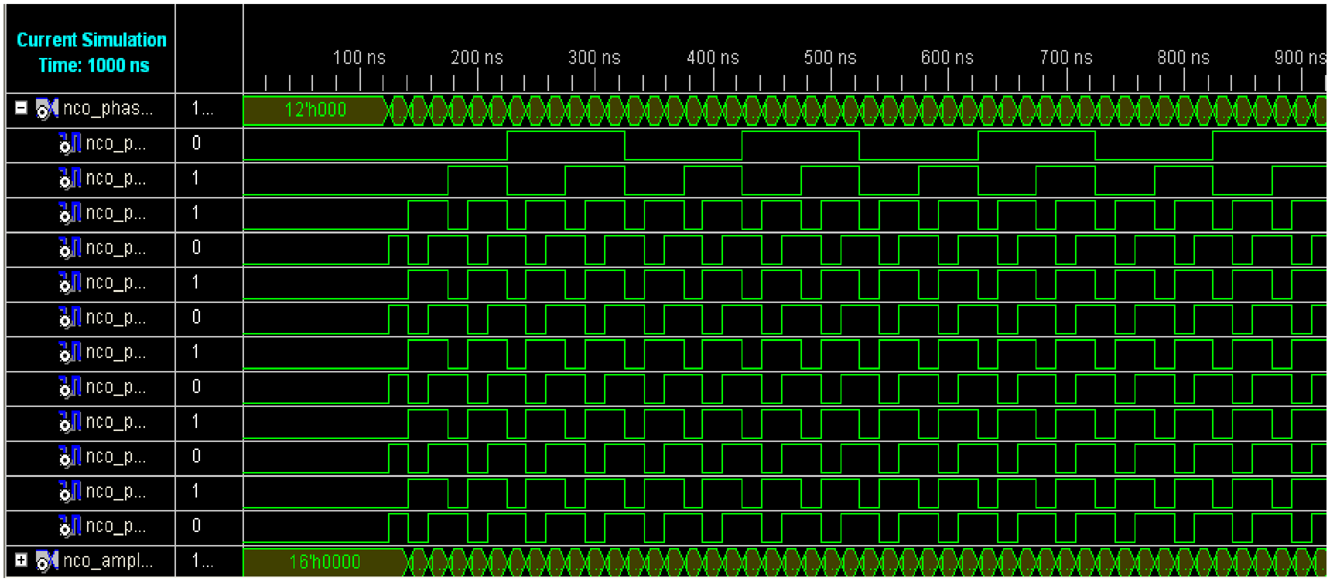
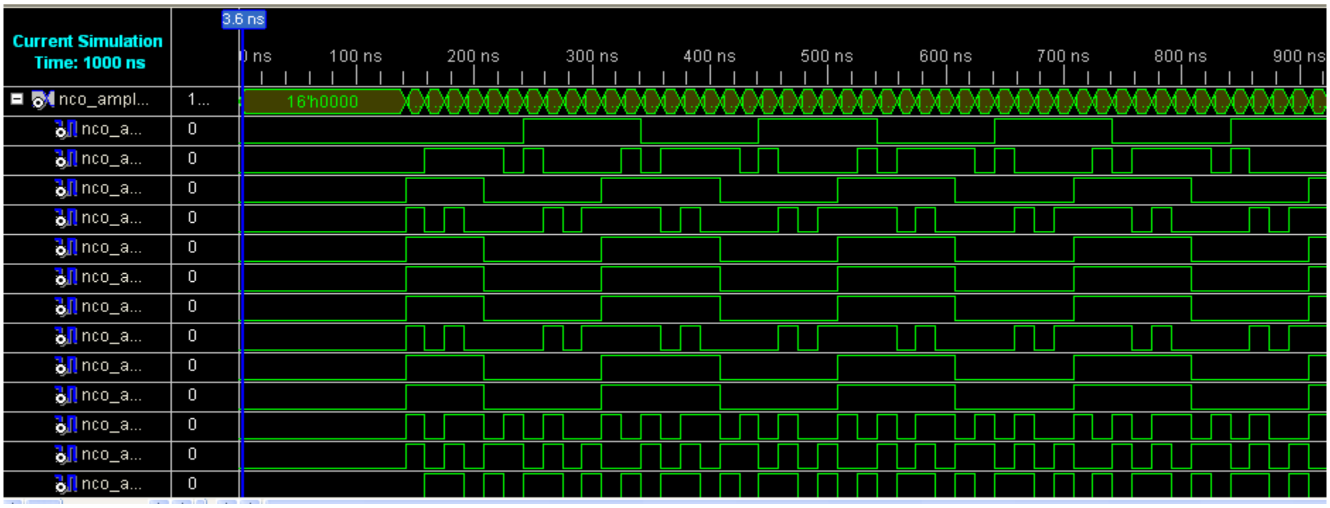


Figure 5: DDS Output at 20 MHz



```
Current Simulation
Time: 1000 ns          100 ns   200 ns   300 ns   400 ns   500 ns   600 ns   700 ns   800 ns   900 ns
nco_phas...    1...    12'h000
  nco_p...     0
  nco_p...     1
  nco_p...     1
  nco_p...     0
  nco_p...     1
  nco_p...     0
  nco_p...     1
  nco_p...     0
  nco_p...     1
  nco_p...     0
  nco_p...     1
  nco_p...     0
nco_ampl...    1...    16'h0000
```

Figure 6: Phase Simulation of DDS



```
                       3.6 ns
Current Simulation
Time: 1000 ns          0 ns   100 ns   200 ns   300 ns   400 ns   500 ns   600 ns   700 ns   800 ns   900 ns
nco_ampl...    1...    16'h0000
  nco_a...     0
  nco_a...     0
  nco_a...     0
  nco_a...     0
  nco_a...     0
  nco_a...     0
  nco_a...     0
  nco_a...     0
  nco_a...     0
  nco_a...     0
  nco_a...     0
  nco_a...     0
  nco_a...     0
```

Figure 7: Amplitude Simulation of DDS

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designed module the frequency at runtime is assigned (see table II). The frequency generated is exactly match the actual frequency which is attained by the simulation. The phase and Amplitude simulations are attained in Xilinx using VHDL shown in figure 6 and figure 7. Direct Digital Synthesizer (DDS) is developed in VHDL using Xilinx ISE. During synthesis, VHDL Script becomes Netlist files that are accepted as inputs to implementation step. VHDL is a high-level language similar to the computer programming language which is intended to support the design, verification, synthesis and testing of hardware designs. It also supports inclusion of technology-specific modules for most efficient synthesis to FPGAs.

C. Design Appraoch

For rapid testing, such designs can be loaded on to the target FPGAs and tested by applying test inputs and directly observing their outputs shown in figure 8. As the complexity of the design under test increases, so does the impracticality of attaching test equipment probes to these devices under test. Here, the Chipscope Pro tools integrate key logic analyzer and other test and measurement hardware components with the target design inside the FPGA. This also improves the frequency of operation.

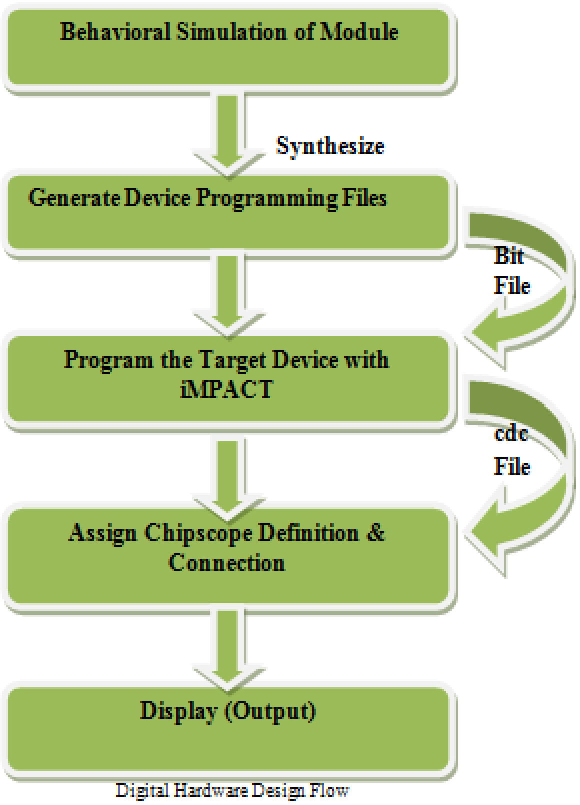
Behavioral Simulation of Module
Synthesize
Generate Device Programming Files
Bit File
Program the Target Device with iMPACT
cdc File
Assign Chipscope Definition & Connection
Display (Output)
Digital Hardware Design Flow

Figure 8: Digital Hardware Design Flow Chart

D. Automated Floating- to Fixed-point Generation

MATLAB algorithms are implemented in fixed-point hardware to achieve higher performance in FPGAs. The output of DDS generated by testbench is displayed with DSP tool, the result is as a periodic waveform with its frequency spectrum as shown in figure 9 & figure 10.

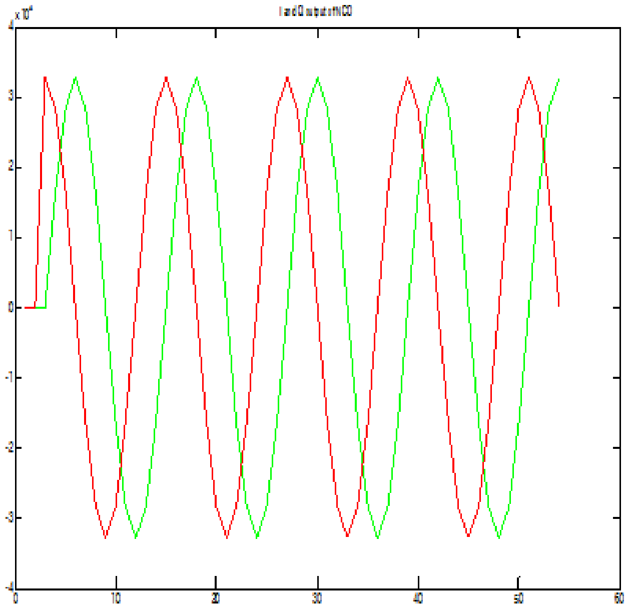

Figure 9: Output of DDS at 5MHz

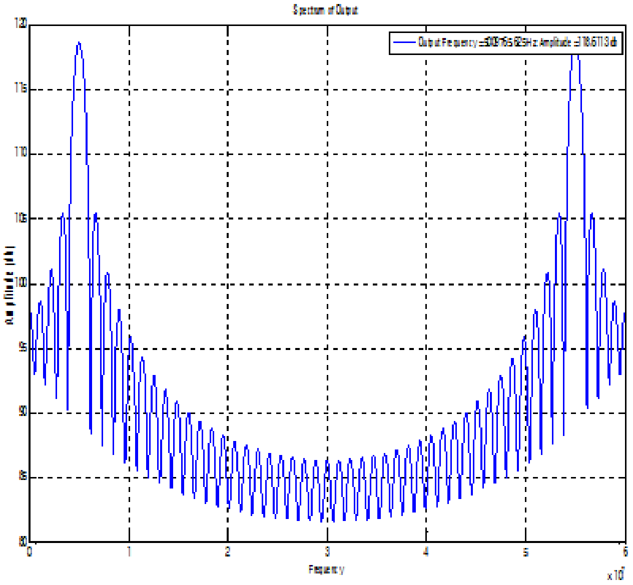

Figure 10: Frequency Spectrum Output of DDS at 5 MHz

IV. Conclusion

The design of Direct Digital Synthesizer is implemented on Virtex II Pro, where MATLAB algorithm is used Floating to fixed point arithmetic to achieve higher and optimal performance of FPGA. This is helpful in the scaling and precision of each variable to be defined to avoid overflow/underflow conditions – a tedious, error-prone process. In this design, maximum output frequency is exactly equal to clock frequency and also the digital sine wave has pure spectral components without distortion.

V. Future Work

In the future scope of work the performance and efficiency of the DDS is further improved by implementing low-complexity algorithm on reconfigurable FPGA.

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